

R E M A R K S

No fee is required for the present amendment under 37 CFR 1.116. Claims 18 to 21, 25, 28, 29 and 31 have been rewritten. Claim 8 and allowed claims 9 to 13 have been retained. Allowable claim 14 has been rewritten in independent form as new claim 34. Claims 1-6, 15-17, 22-24, 26, 27 and 30 have been cancelled without prejudice. Three of these fifteen cancelled claims are independent. Only one independent claim has been added. Thus, upon entry of the present proposed amendment, the total number of claims and the total number of independent claims would be reduced (no fee) and the claims remaining in the case would then be claims 7-13, 18-21, 25, 28, 29, 31 and 34. Note that previously proposed claims 32 and 33 and other claims presented in the proposed amendment of December 5, 2001, were not entered and can therefore be ignored.

Counsel for applicants regrets the unfortunate delay in completing the present amendment and hopes that it will not hinder his efforts to achieve an early and satisfactory disposition of this case. Due to unexpected events it became necessary to defer and postpone action and give priority to other pressing matters.

It is also unfortunate that counsel has found it necessary to seek a rare and unusual remedy which in normal circumstances might seem drastic and inappropriate. As explained hereinafter, strong action was required because of a major mistake by the Examiner that has created an intolerable situation of a rare and extraordinary nature. The rejection of most of the

appealed claims under 35 USC 102 as being fully anticipated by a prior art patent (so irrelevant that it should never have been cited) combined with an unexplained failure to consider and give an action on one of the more specific and most important claims (claim 31) may be unique.

The error of the Examiner in relying on the IBM Flitsch Patent in every one of the prior art rejections in the present case is a major one but is certainly understandable and perhaps excusable because of unusual aspects of the Flitsch patent that may tend to confuse persons not familiar with the technology (e.g., the WET processing of the silicon wafers by a deionized water rinse to remove offending mobile sodium ions). Innocent mistakes are common and to be expected now and then. They usually can be corrected to avoid substantial harm. In the present case, the major error can and will likely be rectified in a satisfactory and amicable manner.

It would be unreasonable to expect an ordinary person, such as a patent examiner, with little knowledge or experience in a highly technical field such as the fabrication of micro-electronic devices, to know that DRY methods for eliminating sub-micron contaminant particles from the surface of silicon wafers are radically and fundamentally different from WET wafer cleaning methods. Persons with experience and expertise in the semiconductor field would know this and immediately recognize the fact that the DRY wafer treating process of the cited Flitsch patent that employs a corona gun and IBM's corona discharge technique to control and remove highly mobile sodium ions in a

wafer heated up to 300°C has no relevance whatsoever when determining the patentability of a wet wafer cleaning process. A typical patent examiner lacks such knowledge and experience and can easily misread a patent dealing with complex technology.

In the discussion which follows it is explained why there is no bona fide or legitimate issue to be presented to the Board of Appeals, why applicant is entitled to a complete action on claim 31 as required by Rule 105, and why the untenable rejection under 35 USC 102 must be withdrawn. The importance and pioneer nature of the invention is also explained in some detail. The presentation of rewritten claims and all of the essential information in the present amendment is intended to simplify the Examiner's task and facilitate an early and satisfactory resolution of the issues.

Applicant's counsel regrets the delay in submitting the present amendment and his inability to complete his review of this case at an earlier date. Unfortunately he presently has a very heavy workload and has been compelled to postpone work on the present case and devote a great deal of his time to other important pressing work that had priority. The unfortunate delay in the present case is the result of unexpected circumstances and was not anticipated. My advanced age is a substantial handicap when speedy action is desired, but I do not see how substantial delay could have been avoided in this case. No one else was available to act in my place or to provide competent and valuable assistance. I am a sole practitioner with long experience and a

high degree of proficiency in the semiconductor field and the only person now available and properly qualified to prosecute the present case.

I acknowledge the fact that the delay may be to some extent bothersome or discommodious in the unusual circumstances of the present case. Perhaps I am partially at fault for failing to spend more time on this case and in underestimating potential problems. If so, I am sorry and will do my best to rectify the situation and hopefully to resolve the problems in a mutually satisfactory manner.

Applicant's counsel also regrets the fact that he has found it necessary to insist on compliance with 37 CFR 1.105 and correction of major errors. He is naturally reluctant to take such drastic action, but believes that it is justified in the rare and extraordinary circumstances of this case as explained in some detail hereinafter. There is no question that applicant is entitled to fair treatment including an action on pending claim 31 whether or not the examiner's oversight was inadvertent.

Counsel can empathize with the ordinary patent examiner and understands the problems he faces because of his own experiences during 4 years as a patent examiner more than 40 years ago and also because of his extensive prosecution of patent applications for the last four decades. An examiner should not become upset or overly concerned about innocent oversights or mistakes that are bound to occur on occasion due to time constraints, inexperience and lack of familiarity with new

technology. Because most patent examiners deal with a wide variety of subjects and do not focus on one specific area of technology, they are naturally handicapped by inexperience and lack of expertise.

During my years as a patent examiner I made many mistakes but in most cases they did little harm because I responded to criticism, usually with special effort to protect my reputation. Because my supervisor read almost all correspondence from my division, I had reason to be careful. That is not to say that I did not skim or gloss over major parts of a patent application and prior art patents in order to conserve valuable time, increase the number of disposals, and meet expected quotas. To be efficient, an examiner is forced to take short cuts and cannot spend too much time on one case to make the "complete" action required by Rule 105. That rule has been in effect for the last 50 years and has been interpreted in a reasonable manner so that applicants usually received fair treatment. Major complaints based on failure to comply with Rule 105 are rare and should be unnecessary when examiners are supervised properly. Major errors can usually be rectified without becoming involved with the more troublesome aspects of the adversarial system of justice.

The major errors in this case would have been avoided if applicant's arguments had been considered with proper care.

The Manual of Patent Examining Procedure (MPEP) and 37 CFR 1.105 (Rule 105) indicate that an Office action rejecting

claims must be complete as to all matters (and all claims) and must include a response to each of applicant's arguments relating to such rejection. The rare and unfortunate situation in the present case where all of the prior art rejections are based on the same irrelevant patent should never have arisen and perhaps would have been avoided if the Examiner had properly replied to the arguments submitted by applicant's counsel.

In the response to the Office action of May 23, 2001, submitted on September 19, 2001 (one week after the 9/11 disaster at the World Trade Center) counsel pointed out that the IBM Flitsch Patent No. 6,136,669 did not suggest applicant's process for wet cleaning of semiconductor wafers and that the corona discharge process described in that patent "cannot satisfy or meet the terms of any of the claims now presented in this case."

The response of 9/19/2001 pointed out (page 3) that the Examiner's description of the Flitsch patent was inaccurate or incorrect, that the patent is not pertinent to the claimed invention and does not suggest a wet cleaning process carried out at a temperature of from 70° to 100°C, and that (page 3, at the bottom) the Flitsch process employs a much higher temperature (i.e., "The wafer 112 . . . is subjected to bias-temperature conditions of IMV/cm at 200°C to 300°C for 2 to 3 minutes.") It is, of course, impossible to perform a WET wafer cleaning operation at a temperature of 200°C or higher. The response (page 6) pointed out that the combination of references

(modifying Flitsch) "fails to fully meet the terms of . . . claims 5, 19, 25 and 28-30 . . . which require charging of the wafers during chemical treatments." Pages 2, 4 and 5 of the response point out that new claim 31 relates to the removal of particulates of sub 0.05-micron size during wet processing of the silicon wafers in 5-tank or 7-tank wet benches as described on page 21 of the specification, that the IBM Flitsch patent '669 does not suggest applicant's wet wafer cleaning process to remove and repel particulates of sub 0.1-micron size, that the Flitsch patent "does not disclose a process capable of removing such fine particles", and that nothing in the patents to Flitsch and Kishii suggest a method capable of removing sub 0.05-micron "killer" particles. It is manifest, of course, that the wet wafer cleaning process of the present invention is concerned with removal of "killer" particles (e.g., in the size range of from 0.02 to 0.1 micron) rather than mobile alkali ions as in the IBM Flitsch patent.

After a brief review of Flitsch Patent No. 6,136,669, it should be self-evident that it is in no way pertinent to applicant's WET wafer cleaning process.

The problems caused by mobile ions are discussed in detail in the article by M. Kuhn entitled "Ionic Contamination and Transport of Mobile Ions in MOS Structure", J. Electrochem. Soc., vol. 118, p. 966 (1971). In the manufacture of semiconductor microelectronic devices, such as MOS integrated

circuits, mobile sodium ions occur in the oxide layers of MOS devices and are detrimental to device performance. In silicon field-effect transistors (FET), for example, mobile ions in the gate oxide layer cause shifts in the operating voltage of the device as explained in U.S. Patent No. 4,978,915.

Flitsch Patent No. 6,136,669, the patent relied on by the Examiner in rejecting the appealed claims, discusses this problem at column 1, lines 20 to 24 and states "Over time, device operation causes mobile ions to move through the gate oxide layer causing operational device functional characteristic variations, such as device threshold voltage shifts, subthreshold leakage and impaired device isolation. Circuits with ion affected devices become unstable."

The purpose of the invention disclosed in the Flitsch patent is to improve semiconductor device stability by removal of mobile alkali ions contaminating the semiconductor chip oxide and insulating layers. This is accomplished by applying a corona discharge bias to the insulating layer that creates an electric charge opposite in polarity to the mobile ions of the insulating layer (See claim 1 of the patent).

As shown in figure 3A of the patent (after the gate oxidation step 100 of the flow diagram shown in Figure 2), a corona discharge gun of the type disclosed in Verkuil Patent No. 5,498,974 generates a corona bias which is directed to the semiconductor wafer 112 and creates an electric charge on the

wafer surface. Step 102 of the Flitsch process (shown and described in Figure 2) is described at column 3, lines 64 to 66 as follows:

"The wafer 112, represented by device structure, is held on a wafer chuck, where it is subjected to bias-temperature conditions of -1MV/cm at 200°C to 300°C for 2 to 3 minutes."

Step 102 of Figure 2 is followed by step 104, a DI water rinse to remove both the corona charge and the mobile ions.

Thus it is crystal clear that the electric charge is applied while the wafer is dry (Water has a boiling point of 100°C and cannot exist in the liquid phase at a temperature of 200°C or more).

The invention of Flitsch can be readily understood by carefully considering the drawings of his Patent No. 6,136,669 and the description thereof at column 1, lines 33 to 60, which is quoted below.

"FIGS. 1A-C show mobile ions being formed in a cross section of a semiconductor wafer during typical prior art semiconductor manufacturing steps, field effect transistor (FET) manufacturing steps in this example . . . A thin gate oxide layer 56 is formed over the semiconductor layer 50."

"FIG. 1B is an expanded view at a typical device region 52. In the expanded view of FIG. 1B, mobile ions 58 (Q_m) are trapped in the thick insulator 54 and thin gate oxide 56. In this example, the mobile ions 58 are primarily positively charged ions, and primarily at the semiconductor-isolator interface

(e.g., the oxide-silicon interface). . . . Mobile ions 58 remain in the structure as a result of prior processing steps."

"In FIG. 1C, a gate 60 (e.g., polysilicon), is formed on the structure of FIG. 1B."

"Under normal device operation, bias voltages on the gate 60 eventually force the mobile ions 58 through the gate oxide 56'. The movement of these mobile ions 58 alters the FET's threshold voltage (V_T), making the FET unstable, in effect, giving the FET a time varying V_T ."

All of the claims of the present Loxley patent application require the electric charge to be applied during wet processing while the wafer is wet (not dry). There is no bona fide or legitimate issue in the present case for adjudication by the Board of Appeals. The Flitsch patent is in no way pertinent to the claims of the present Loxley application. There is no basis whatsoever for the rejection of claims 1, 2, 4, 8, 18, 21, 26 and 28 as being anticipated by Flitsch Patent No. 6,136,669 under 35 USC 102. That rejection is not legitimate and must, of course, be withdrawn in the facts of this case. A theoretical alternative (not possible in this case) is a bona fide effort to explain a basis for the rejection (there is none) and to comply fully with 37CFR1.105 and MPEP Section 707.07 and the high standards expected by the Board of Appeals.

The appealed claims are clear and definite. It appears that important limitations have been overlooked or misunderstood.

It appears that some discussion regarding the scope of the claims and the meaning and significance of the terminology

used in the claims is necessary or desirable and that significant limitations have been overlooked or misunderstood. Examples of language used in the claims are "charged during rinsing", "charged during wet processing", "particles bonded to the wafer surface", "submicron killer particles", "submicron particulates" (claim 15) and "harmful sub 0.05-micron particles." Of concern are statements, for example, on pages 2 and 4 of the final Office action that ions (i.e., mobile alkali ions) are particles smaller than 0.1 micron and that "features upon which applicant relies are not recited in the rejected claims."

The rejected claims are clear and definite and use terms whose meanings could not be misunderstood by persons familiar with the art. As pointed out on pages 3 and 31 of the specification, the terminology employed in the present application is to be construed as consistent with that used in the most authoritative textbooks relating to the processing of silicon semiconductor wafers, namely "Handbook of Semiconductor Wafer Cleaning Technology" by Werner Kern and "Microchip Fabrication" by Peter Van Zant.

Pages 201 and 203 of Kern's 1993 handbook indicates that there are two types of wafer cleaning processes in commercial use. They are liquid phase, or wet, wafer cleaning processes and gas-phase, or dry, wafer cleaning processes. The vast majority are wet processes. As stated "In general, it is not expected that dry cleaning will replace wet cleaning . . .

much needs to be accomplished to make it [dry cleaning] fully compatible with large scale industrial production." Today, wet wafer cleaning is the most frequently applied processing step in microchip fabrication. Dry cleaning is seldom used and is not needed and not used in the typical 360-step manufacturing process described on pages B-3 to B-14 of the SEMATECH publication referred to on page 3 of this application.

The word "wet" has become a well-established term of art whose meaning is unmistakable. In Flitsch Patent No. 6,136,669, for example, there can be no problem determining the meaning of "wet chemical process steps" (col. 1, line 27), "wet step" (col. 3, line 19; col. 4, line 33), "wet wafer preclean" (col. 4, line 36) or "wet process step" (col. 6, line 24).

The term "wet" is also a temperature limitation because water (b.p. 100°C) or an aqueous liquid cannot remain in the liquid state at a temperature substantially above the boiling point. In the Flitsch patent the corona charge is applied to a DRY wafer at a temperature of 200°C before the subsequent water rinse. Column 3, lines 15 to 20 of the patent, indicates that the corona bias-temperature step to remove mobile [sodium] ions is carried out BEFORE proceeding with a WET step. The Loxley invention as defined in the rejected claims requires applying an electric charge to the wafer face DURING (not before) the wet processing step. The Flitsch patent is nonanalogous and in no way pertinent to the Loxley invention. The 35USC102 "anticipation" rejection based on Flitsch makes no sense.

The word "particulates" has also become a well-established term of art and is clearly defined in the Van Zant textbook "Microchip Fabrication" (Second Edition) referred to on page 3 of the present application. Pertinent portions from page 146 of that textbook are quoted below.

"Wafer surfaces can have four different types of contamination . . . The four types are

1. Particulates
2. Organic residues
3. Inorganic residues
4. Unwanted oxide layers

"Particulates on the wafer surface vary from large ones (50-micron size) to very strong ones about a micron in size . . . The smaller particulates are more difficult to remove because they are held to the surface by strong intermolecular forces."

"Particulates is a term of art concerned with solid particles and in no way includes subatomic particles or mobile ions of the type described in the Flitsch patent. It is manifest that the term "particulate" as used, for example, in original claims 7 and 21 and defined on pages 24 and 25 of the specification and the term "killer particles" or "killer defect" as used, for example, in original claim 8 and defined at pages 4, 5 and 10 of the specification, relate to solid particles, not ions. It is also clear that the term "particle" is used in the present application in the normal sense as customarily used in the semiconductor industry in connection with particulate contamination. A mobile ion, such as a sodium ion can in no way be considered a "particle" as that term is used in the specification and claims of the present application. In the field of wafer fabrication and wafer cleaning, the terms "particles" and "particulates" are, of course, synonymous.

As to Claim 31, Compliance with Rule 105 is Mandatory

MPEP Section 707.07 and 37 CFR 1.105 clearly indicate the requirements for completeness and clarity in an Office action. The action must be "complete as to all matters" and all pending claims and the "examiner must address all arguments" including any arguments relevant to the references being applied.

As stated in MPEP Section 706.07 "The examiner should never lose sight of the fact that in every case the applicant is entitled to a full and fair hearing, and that a clear issue between applicant and examiner should be developed." Prosecution of a patent application must be "consistent with a thorough consideration of its merits."

Unfortunately no bona fide or legitimate issue has been reached that could justify submission of this case to the Board of Appeals. In any event applicant is entitled to an action by the Examiner on overlooked claim 31.

At first glance pending claim 31 might seem to be an insignificant dependent claim not requiring independent consideration. Overlooking this one claim may appear to be a minor omission of little consequence, but such a conclusion would be completely wrong. The failure to give proper consideration to claim 31 was a major mistake with major adverse consequences for applicant. Claim 31 is a very important claim that sets forth features not remotely suggested by the prior art.

The erroneous rejection of many claims as being anticipated by Flitsch Patent No. 6,136,669 could perhaps be characterized as excusable inadvertence due to inexperience and

lack of familiarity with the technology. However, at the present time, faced with the truth, any rejection of claim 31 based on the irrelevant and inapplicable corona discharge method of the Flitsch patent would be unthinkable. It would be utterly impossible to provide a rational argument in support of such a rejection.

The presentation of rewritten amended claims in the present amendment should help the Examiner in his consideration of claim 31 and his reconsideration of the unfortunate rejection of the claims under 35 USC 102. Claim 31 is dependent on claim 18 which is specific in defining a fabrication process wherein "the wafer is wetted and repeatedly subjected to wet cleaning, rinsing and drying operations to remove contaminants" and "charged during wet processing to provide an effective field intensity . . . sufficient to facilitate removal of harmful sub 0.05-micron particulates bonded to the wafer surface."

Claim 31 is more specific than base claim 18 in defining a wafer fabrication process "wherein a row of 10 or more silicon wafers is supported in a vessel or wafer carrier" during the wet cleaning operations. This feature of the wet cleaning operation has astounding ramifications and advantages. Killer particles in the dangerous size range of 0.03 to 0.1 microns can be readily eliminated in a simple mass production system wherein a row of 20 to 30 or more parallel closely-spaced wet silicon wafers of large diameter are cleaned simultaneously in an aqueous liquid and are uniformly charged by induction to avoid harmful electrolysis. This unique combination is a godsend to the

semiconductor industry and not remotely suggested by the prior art. Heretofore, the industry had no practical method for eliminating sub 0.1-micron particulate contaminants (e.g., "killer defects") in the manufacture of advanced microchips. Applicant's solution to the problem is astounding because it is simple, inexpensive and remarkably effective. It is a pioneer invention in spite of its simplicity in retrospect. As stated by America's foremost patent jurist, Learned Hand "It is the obvious, put to use, that most often proves invention."

Further discussion regarding the Flitsch (IBM) Patent No. 6,136,669 and the corona discharge method may be helpful to explain why it is impossible to provide a rational argument in support of a rejection based on that patent. Attention is directed to the related IBM Patent No. 6,060,709 to Verkuil. Both the IBM Flitsch patent '669 and the IBM Verkuil patent '709 use a corona gun as disclosed in earlier IBM Verkuil Patent No. 5,498,974 and incorporate the entire disclosure of that earlier patent by reference. Both patents deposit a corona charge on a dry silicon semiconductor wafer. As pointed out in the more recent IBM Verkuil patent '709, the application of the electric corona charge while the wafer is dry can eliminate both the (wet) rinsing step and the necessary drying step (after rinsing). As stated in the IBM patent ('709):

"For example, it is common to rinse a wafer in water to remove any charge that has accumulated on the oxide layer formed on the surface of the wafer. Such a rinsing entails not only the rinsing step, but also, a drying step. This increases the chances for contamination and damage of the wafer. In addition, the drying process may reintroduce charge gradients."

No one can deny that the corona gun of the three IBM patents ('974, '669 and '709) applies the corona charge to a DRY wafer and would be completely inoperative with respect to a wet wafer or a submerged wafer because water would remove any charge. In other words the corona gun of the IBM patents and the corona discharge method for charging a dry semiconductor wafer has no utility whatsoever in the wet processing of wafers. The Flitsch patent is completely irrelevant with respect to applicant's claim 31 directed to a process wherein the face of each silicon wafer is electrically charged during wet processing while a row of 10 or more closely spaced wafers is supported in a wafer carrier during such wet cleaning operations (i.e., while 10 to 30 or more wafers are submerged in an aqueous liquid).

There is no rational basis for arguing that the corona discharge method of the IBM Flitsch patent '669 is in any way pertinent to claim 31. The process of claim 31 is inoperative and has no utility in the absence of water. A corona gun as disclosed in the Flitsch patent cannot apply a charge to each of the 10 to 20 or more silicon wafers in a row. Where would the gun be located? How could it possibly work under water or even in the absence of water. A complete action on claim 31 would require a clear explanation as to all of these points if a rejection of the claim is based on the Flitsch patent. This would be impossible.

The present case discloses a pioneer invention that is a godsend to the semiconductor industry. Full, fair and complete consideration of the merits is in order.

The Examiner's favorable action as to claims 9 to 13 and claim 14 (now rewritten in independent form as claim 34) is commendable, but his reluctance to allow other claims based on the irrelevant Flitsch patent is not understood. The discussion which follows may be helpful in finding a satisfactory resolution of the problems in this case and showing why the present invention is of a pioneer nature deserving careful consideration.

A few admonitions would seem to be in order regarding compliance with the rules and the basic burdens to be carried when rejecting claims. Attention is directed to the various requirements of MPEP Section 706.02 and the fact that an examiner must cite the BEST available prior art (Flitsch is not even pertinent). An examiner should also be aware that the law places a heavy burden on the Patent Office to justify the rejection of a patent claim.

The burden is on the Commissioner to establish that the applicant is not entitled to a patent. The Patent Office is required to produce the factual basis for its rejection of patent claims under 35 USC 102 or 103. (In re Warner, 379 F2d 1011, 1016, 154 USPQ 173,177; Graham v. John Deere, 383 US 1, 148 USPQ 459). This includes the provision of evidence of a motivating force which would impel a person skilled in the art to do what applicant has done.

The present invention relates to wet processing of semiconductor wafers and more particularly to a special wafer cleaning system that is effective in removing colloidal- or sub 0.1-micron size particles that cannot be removed effectively by any known prior-art process.

The RCA-type wafer cleaning methods of Werner Kern that have been standard in the semiconductor industry for more than a quarter of a century have been improved substantially during the last decade by use of megasonic transducer means. Improved megasonic cleaning means can remove particles as small as 0.15 micron. However, such wet cleaning techniques are not effective in removing extremely small sub 0.1-micron particles (e.g., those with a particle size below 0.07 micron).

Heretofore the semiconductor industry was convinced that wet cleaning methods would never be effective in removing such small or colloidal-size contaminant particles. The best scientific minds grappling with the problem assumed, with good reason, that the tremendous van der Waals adhesive forces acting on colloidal-size particles at the wafer surface could not be overcome and that elimination of such particles by a simple wet cleaning operation was virtually impossible. The experts were convinced that the only real hope for success was a breakthrough or major improvement in dry wafer cleaning technology, perhaps a sophisticated laser technique.

The present invention provides the needed breakthrough and eliminates the need for a drastic switch from the usual wet cleaning systems to a new dry system. It involves the amazing

discovery that colloidal-size particles and sub 0.05-micron particles bonded to a wafer surface containing delicate microcircuits can easily be removed and repelled when the wafer is negatively charged in a suitable manner by applying a relatively small or limited voltage, such as 10 to 40 volts or more, insufficient to damage or degrade vulnerable portions of the microcircuits or significantly reduce the yield of top-quality microchips.

In the semiconductor industry, one of the current target goals in microchip fabrication is to reduce the defect density to less than 0.03 defects per square centimeter. An object of the present invention is to reach that goal in a simple and effective manner by substantially eliminating "killer particles" (e.g., with a particle size in the range of from 0.03 to 0.09 micron) and minimizing the number of troublesome particles (e.g., those with a particle size more than 10 percent of the minimum line width or feature size) which are detrimental or highly undesirable.

The term "killer defect" is used herein in the broad sense to cover an unacceptable or intolerable defect in the microelectronic circuits of a semiconductor device or microchip caused by a contaminant particle trapped or embedded in the device during the fabrication process.

The term "killer defect" is used in a narrow sense in Table 1 on page 5 of this specification to describe trapped or embedded particles with a particle size that is at least about 20 percent of the minimum line width or feature size (identified in the table as "Min. dimension"). That table from the SEMATECH road

map indicates that one of the goals is to obtain a 90-percent yield of advanced (0.25 um) wafers with no more than 0.03 killer defects per square centimeter.

For the last 30 years the most competent scientists have been convinced that the primary force binding a colloidal-size particle to a wafer surface is van der Waals attraction which is universal and dominating when separation distances between a particle and a surface are extremely small (e.g., below 5 nanometers). The forces of attraction increase as the particle size decreases so that it appears virtually impossible to overcome the van der Waals forces when the particle size is 0.01 micron or less.

On this basis foremost experts, such as RCA's Werner Kern, concluded that wet cleaning processes could not provide a satisfactory way to remove colloidal-size particles when manufacturing the most advanced microchips and that new dry methods would have to be developed.

Attempts were made to improve the effectiveness of wet wafer cleaning processes by causing strong or violent agitation of the liquid as by providing bursts of energy from megasonic transducers. However, such methods were not adequate for removal of sub 0.1-micron particles. Heretofore, more sophisticated dry cleaning methods seemed to provide the only real hope for minimizing particulate contamination when manufacturing advanced microprocessors with a minimum feature size or line width of 0.15 micron or less.

The unique wet wafer cleaning system of the present invention is a godsend to the semiconductor industry, which heretofore had no practical and effective way to eliminate "killer" particles of sub 0.1-micron size or to reach target defect-density goals, such as those set forth in Table 1 on page 5 of the present application.

There is no bona fide or legitimate issue in this case that could justify review by the Board of Appeals.

The simple fact (as fully explained herein) is that every one of the rejections set forth in the final Office action are baseless and hinge on or depend almost entirely on a single prior art patent (Flitsch 6,136,669) that is totally inapposite and has nothing to do with the subject matter of the appealed claims. The patent is irrelevant, of no interest, and should never have been cited. An unpleasant confrontation with this simple truth cannot be avoided.

The peculiar and incredible situation that has arisen in this case is rare and quite extraordinary, if not unprecedented. Under these circumstances, applicant's counsel is forced to seek appropriate relief that might otherwise seem drastic. This is not to say that reasonable people cannot deal with the problem in a simple and amiable manner or that the Examiner cannot rectify the matter in a reasonable way.

As explained previously, applicant is entitled to an action on overlooked claim 31 that necessarily requires a study of the irrelevant Flitsch patent. A rejection of claim 31 based on a reaffirmation of Flitsch is unthinkable and not going to happen.

The Examiner will, of course, have to reconsider the rejection under 35 USC 102 which obviously cannot stand.

In any event, it would be unconscionable to require applicant to file an appeal brief if the Examiner knows he cannot defend his rejection in an Examiner's Answer.

Counsel would like to discuss this case with the Examiner at an early date after he has the opportunity to consider the present remarks and before he takes further action.

Respectfully submitted,

Vincent A. Greene

Vincent A. Greene
Registration No. 17,389
25931 Euclid Ave., Suite 116
Cleveland, Ohio 44132
Telephone: (216) 481-7772

June 19, 2002

RECEIVED
JUL - 1 2002
TECHNOLOGY CENTER 2800

Serial No. 09/490,162

Version with Markings to Show Changes Made

18. (Amended) In a [A] process of the character described for fabrication of microelectronic devices on silicon wafers wherein microcircuits are formed on the front face of a wafer by a plurality of layering, patterning, doping and heating operations and the wafer is wetted and repeatedly subjected to cleaning, rinsing and drying operations to remove contaminants, [characterized in that] the improvement wherein said front face of the process wafer is artificially charged during wet processing to provide an effective field intensity and [with] a negative voltage of at least 2 volts sufficient to facilitate removal of harmful sub [0.1] 0.05-micron [contaminant particles] particulates bonded to the wafer surface [during the wet cleaning operations].

7. (Amended) A process according to claim [1] 18 wherein particulate contaminants are removed and substantially eliminated from a wafer by charging the wafer with a negative voltage of from about 2 to about 60 volts while providing a field intensity of at least 0.02 volts/mm at the wafer surface sufficient to dislodge, remove and repel substantially all of the harmful sub 0.1-micron [particles] particulates.

-- 19. (Amended) A process according to claim 18 wherein the front face of the process wafer is subjected to wet CMP polishing [with colloidal silica or alumina particles having an

Version with Markings to Show Changes Made

average particle size of from 0.01 to 0.03 microns] and is thereafter subjected to chemical cleaning and DI rinsing operations while said front face is negatively charged to a voltage sufficient to cause [efficient or] substantially complete removal of sub 0.05-micron contaminant particles bonded to the wafer surface.

20. (Amended) A process according to claim [1] 18 [for fabrication of microchips having a minimum line width or circuit image size less than 0.15 microns] wherein the front [fron] face of each wafer is subjected to [the] wet CMP polishing [with colloidal silica or alumina particles] and is thereafter subjected to a wet cleaning operation for 0.5 to 5 minutes while said front face is negatively charged to a [substantial] limited voltage of [such as] 10 to 40 volts or more sufficient to [remove] cause substantially complete removal of [colloidal or] sub 0.05-micron [contaminant] killer particles, the voltage and rate of [large] charge of the wafer surface being applied or controlled during said wet cleaning operation in such manner as to minimize or limit damage or alteration of the delicate microcircuitry.

21. (Amended) A process according to claim 18 wherein particulate contaminants are removed and substantially eliminated from a wafer by [In a process of the character described for forming delicate microcircuits on the front face of a semiconductor wafer wherein the wafer is subjected to a large

Version with Markings to Show Changes Made

number of layering, patterning and doping operations and many wet processing steps to remove organic, metallic and particulate contaminants, the improvement in which] providing the front face of the wafer [is provided] with a limited electric charge [of at least 2 volts] during wet processing steps insufficient to degrade the microcircuits, the charge being sufficient to provide a field intensity at said front face effective to dislodge and remove sub [0.1] 0.5-micron [particles] particulates bonded at the wafer surface.

25. (Amended) A process according to claim [24] 18 wherein the front face of the wafer is charged to a field intensity of at least 0.02 volts/mm during washing of the wafer in a highly dilute alkaline solution.

28. (Amended) A process according to claim [26] 18 wherein said [wafer] front face is provided with a limited electric charge of at least 10 volts during most of said wet cleaning [steps] operations to minimize particulate contamination.

29. (Amended) In the manufacture of advanced microchips from flat semiconductor wafers having delicate microcircuits formed on one face, an RCA-type wet cleaning process wherein a single wafer is treated in an aqueous alkaline solution containing hydrogen peroxide and thereafter treated in an acidic solution, rinsed in pure water and dried, characterized in that the wafer surface containing said delicate microcircuits

Version with Markings to Show Changes Made

is electrically charged during the wet cleaning process to cause effective removal of sub 0.05-micron killer particles that are [strongly] bonded to the wafer face.

31. (Amended) A process according to claim 18 wherein a row of 10 or more silicon wafers is supported in a vessel or wafer carrier during the cleaning operations, the front face of each wafer being charged to a limited negative voltage, such as 2 to 60 volts, insufficient to harm the delicate microcircuits formed on that face and having a field intensity of at least 0.02 volts/mm sufficient to cause efficient removal of harmful sub 0.05-micron particulates [particles].